**WHAT IS CLAIMED IS:**

1. A method for exposing one or more areas on a semiconductor wafer to charged particles, comprising:

aligning a wafer mask, having one or more mask patterns thereon, with the semiconductor wafer; and

passing the charged particles through the mask patterns to land on one or more selected areas on the semiconductor wafer.

2. The method of claim 1 wherein the charged particles transform semiconductor materials in the selected areas to have a higher resistivity than other areas not exposed to the charged particles.

3. The method of claim 2 wherein the selected areas become semi-insulating areas after receiving the charged particles with a collective energy level exceeding a predetermined threshold.

4. The method of claim 1 further comprising bonding the semiconductor wafer with the wafer mask before passing the charged particles.

5. The method of claim 1 wherein the wafer mask has one or more alignment patterns thereon for aligning with the semiconductor wafer.

6. The method of claim 1 wherein the mask patterns are openings with their center portions unremoved.

7. The method of claim 6 wherein the openings are in rectangular shape.

8. The method of claim 1 wherein the wafer mask is made from a silicon wafer having a thickness between 100 um to 800 um.

9. The method of claim 1 wherein an angle between sidewalls of the mask patterns

on the wafer mask and the surface of the wafer mask is between 80 to 100 degrees.

10. The method of claim 1 further comprising:

determining the one or more selected areas on the semiconductor wafer for receiving the charged particles; and

generating the wafer mask having the mask patterns contained thereon for passing the charged particles to land on the selected areas when the semiconductor wafer is aligned with the wafer mask.

11. The method of claim 1 wherein the charged particles are protons.

12. The method of claim 1 wherein the charged particles have an energy level between 0.5 to 5 MeV.

13. A method for exposing one or more areas on a semiconductor wafer to charged particles for making semi-insulating areas, comprising:

aligning a wafer mask, having one or more mask patterns thereon, with the semiconductor wafer, with the mask being I predetermined proximity to the semiconductor wafer;

generating the charged particles; and

directing the charged particles through the mask patterns to land on one or more selected areas on the semiconductor wafer,

wherein semiconductor materials in the selected areas of the semiconductor wafer are transformed to have a higher resistivity than those not exposed to the charged particles.

14. The method of claim 13 wherein the selected areas become semi-insulating areas.

15. The method of claim 13 further comprising:

determining one or more selected areas on the semiconductor wafer for receiving the charged particles; and

generating a wafer mask having one or more mask patterns contained thereon for passing

the charged particles.

16. The method of claim 13 further comprising bonding the semiconductor wafer with the wafer mask before passing the charged particles.

17. The method of claim 13 wherein the wafer mask has one or more alignment patterns thereon for aligning with the semiconductor wafer.

18. The method of claim 13 wherein the mask patterns are rectangular openings.

19. The method of claim 13 wherein the mask patterns are rectangular openings with their center portions of wafer material unremoved.

20. The method of claim 13 wherein the wafer mask has a thickness between 110 um to 800 um.

21. The method of claim 13 wherein an angle between sidewalls of the mask patterns on the wafer mask and the surface of the wafer mask is between 80 to 110 degree.

22. The method of claim 13 wherein a fluence of the charge particles is between 1E14 ea/$cm^2$ to 1E17 ea/$cm^2$.

23. The method of claim 13 wherein the charged particles land substantially perpendicularly to the selected area.

24. A system for exposing one or more areas on a semiconductor wafer to charged particles, comprising:

means for aligning a wafer mask, having one or more mask patterns thereon with the semiconductor wafer;

means for generating the charged particles; and

means for directing the charged particles through the mask patterns to land on selected

areas on the semiconductor wafer.

25. The system of claim 24 further comprising means for determining one or more selected areas on the semiconductor wafer for receiving the charged particles.

26. The system of claim 24 further comprising means for bonding the semiconductor wafer with the wafer mask.

27. The system of claim 24 further comprising means for generating the mask patterns for passing the charged particles.

28. The system of claim 27 wherein the means for generating the mask further includes means for generating one or more alignment patterns thereon for aligning with the semiconductor wafer.

29. The system of claim 27 wherein the mask patterns are rectangular openings.

30. The system of claim 27 wherein the mask patterns are rectangular openings with their center portions of wafer material unremoved.

31. The system of claim 24 wherein the means for generating charged particles generates the charged particles with an energy level above 0.5 MeV.

32. The system of claim 24 wherein the means for generating charged particles generates the charged particles with an energy level below 5 MeV.